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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,918	02/24/2004	Naoki Takada	62807-166	1966

7590 08/22/2007

MCDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER
SHERMAN, STEPHEN G

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
08/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/784,918	TAKADA ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-8 and 11-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-8 and 11-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed the 3 July 2007. Claims 1-3, 5-8 and 11-13 are pending. Claims 4, 9-10 and 14-20 have been cancelled.

Response to Arguments

2. Applicant's arguments with respect to claims 1-3 have been considered but are moot in view of the new ground(s) of rejection.

3. Applicant's arguments filed with respect to claims 5-8 and 11-13 have been fully considered but they are not persuasive.

On page 9, under the heading "Claims 4-13 Are Not Anticipated by Nitta", the applicant argues the 35 U.S.C. §102(e) rejection of claim 11. The applicant argues the rejection by stating that there is deterioration of display quality when there is a specific difference of capacitance variation between a gate and a source, and that it is not possible to solve this problem using only the disclosure of Nitta. The applicant then states that Claim 11 recites the limitation "...the control circuit outputs to the data driver blanking data other than the display data in place of the display data at timing at which the second clock signal is created immediately before the timing at which the second clock signal is not created..." The applicant summarizes by stating that this feature is

not taught by Nitta and point to Nitta column 7, line 45 to column 8, line 3. The examiner respectfully disagrees.

First of all, the fact that Nitta does not solve the problem of capacitance variation between a gate and a source is irrelevant to the claimed invention. Nitta does not have to solve the same problem as the applicant, Nitta only needs to anticipate the claims. Next, the applicant states that Nitta does not teach the limitation "...the control circuit outputs to the data driver blanking data other than the display data in place of the display data at timing at which the second clock signal is created immediately before the timing at which the second clock signal is not created..." by citing the portion of Nitta found in column 7, line 45 to column 8, line 3, however, this portion on Nitta does not prove that Nitta does not teach the claimed invention. The applicant did not even respond to the examiner's rejection of this limitation. In the rejection, the examiner stated: "As shown in Figure 4, the point in time in which data B on O-DDR is supplied is immediately before the time when clock CL3 would be created". Figure 4 of Nitta specifically shows the black data B being output, for example when gates G1-G4 are selected at the same time. Immediately after these gate lines G1-G4 are selected, CL3 is NOT created. CL1 is a clock signal which is created on a regular interval which CL3 follows except for when CL3 is not created. It can be noticed by looking at Figure 4 that when CL1 is applied for the fifth time, a pulse for CL3 is NOT created and that at this time when CL3 is not created is immediately after the black data was supplied, i.e. the black data was supplied immediately before CL3 is not created as required by the claim. Thus Nitta anticipates the **CLAIMED INVENTION**.

Claim Objections

4. Claims 5, 7 and 8 are objected to because of the following informalities:

Clam 5 recites: "reads the blanking data from the second memory at timing generating signal just before the timing which is synchronized with the first clock signal", which should be changed to reflect proper English so that the claim is not unclear.

Claim 7 recites: "the scan driver selects n rows of pixels at timing generating signal just before the timing at which", which should be changed to reflect proper English so that the claim is not unclear.

Claim 8 recites: "the scan driver a first scanning enable signal to invalidate selection of the pixels by the scan driver at timing generating signal just before the timing at which the second clock signal is not created and a second scanning enable signal to validate selection of the pixels by the scan driver at timing generating signal just before the timing at which the second clock signal is not created", which should be changed to reflect proper English so that the claim is not unclear.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites limitation "the scan driver selects first n rows (n > 2) of pixels at a time, sequentially selects m rows (m < n) of second n rows of pixels, and selects pixels from the second n rows of pixels a plurality of times for each row during one frame period, then selects the first n rows of pixels and n rows of pixels adjacent the first n rows of pixels at a time, then sequentially selects m rows of pixels for n rows of pixels adjacent the second n rows of pixels and selects n rows of pixels adjacent the second n rows of pixels a plurality of times for each row during one frame period" This limitation renders the claim indefinite because the claim is now referring to both carrying out double gate driving for displaying data and for double gate driving of blanking data, however, Figure 5 is the only figure that shows the double gate driving for the blanking data. Figure 5, however, does not show double gate driving for the display data. Double gate driving for the display data is only shown in Figures 3, 4, 7, 8,9 and 10 but NOT in Figure 5. Therefore it is unclear to the examiner how the double gate driving for

the display data is done with the double gate driving for the blanking data since it in not shown in Figure 5. The specification only states that the double gate driving of the display data is the same as in the first embodiment, i.e. Figure 3 and 4, however, Drawing 5 shows the double gate driving of the black data beginning at lines G1-G4 whereas Figures 3 and 4 show the black data being implemented differently.

Furthermore the claims define that n rows are selected that are adjacent the first n rows, however, as shown in Figures 3 and 4, only G1 and G2 are selected at first. Claim 2 defines that n=4, however, this would not be the case since only 2 gate lines are selected during a period of time. Therefore, since n is defined to be greater than 2 in claim 1 the claim is indefinite because there exists a time when only 2 lines are selected.

Therefore, since Figure 5 does not show the double gate driving of the display data and the specification only refers to the first embodiment the claims are indefinite because the double gate driving of the display data shown in the first embodiment does not comply with the claimed limitations. If there is any explanation as to the claims that the applicant can provide to help with the clarity of the claimed limitations the examiner invites the applicant to do so.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 5-8 and 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Nitta et al. (US 7,027,018)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 11, Nitta et al. disclose a display device, comprising:

a pixels array including a plurality of pixels arranged in a form of a matrix (Figure 3, item 101 is explained to be a pixel array in column 11, lines 61-65.);

a data driver for supplying a tone voltage corresponding to display data to the pixels (Figure 3, item 102 is explained to be data driver in column 12, lines 48-51.);

a scan driver for selecting pixels of at least one row to which the tone voltage is to be supplied (Figure 3, items 103-1 through 103-3 are explained to the scanning drivers in column 12, lines 51-55.); and

a control circuit for controlling the data driver and the scan driver (Figure 3, item 104 which is explain in column 12, lines 61-67.), wherein:

the control circuit outputs a first clock signal and the display data to the data driver (Figure 3 and column 12, lines 61-67 explain that timing signals 107 and display data 1056 are supplied from the control circuit 104 to the data driver 102.);

the control circuit outputs to the scan driver a second clock signal, the second clock signal not being created every n (n >2) signal creation thereof and outputs a scanning start signal generated a plurality of times during one frame period (Figure 3 shows that the control circuit 104 outputs a clock CL3 labeled as 112 to the scanning drivers 103-1 through 103-3. Figure 4 shows that the clock CL3 is not created every 5^{th} signal creation. Column 12, lines 61-67 that the scanning start signal 113 labeled as FLM in the Figures is also outputted by the control circuit 104 to the scanning drivers 103-1 through 103-3.); and

the control circuit outputs to the data driver blanking data other than the display data in place of the display data at timing at which the second clock signal is created immediately before the timing at which the second clock signal is not created (As shown in Figure 4, the point in time in which data B on O-DDR is supplied is immediately before the time when clock CL3 would be created.).

Regarding claim 5, Nitta et al. disclose the display device according to claim 11, further comprising:

a first memory for keeping the display data therein (Column 15, lines 15-25 explain that memory 105 is used to store the display data.); and

a second memory for keeping the blanking data therein (Column 15, lines 25-29 explain that the blanking data are stored in the pixels array, i.e. a second memory different from memory 105.), wherein:

the control circuit reads the display data from the first memory at timing synchronized with the first clock signal, outputs the display data to the data driver, reads the blanking data from the second memory at timing generating signal just before the timing which is synchronized with the first clock signal and at which the second clock signal is not created, and outputs the blanking data to the data driver (As explained above, display data is output in accordance with the clock CL1 and would be output from memory 105, while the blanking data would be output when clock CL3 is not created and would be read from the place where it is stored in the pixel array.).

Regarding claim 6, Nitta et al. disclose the display device according to claim 11, wherein a period of the first clock signal and a period of the second clock signal are synchronized with a scanning period for the scan driver to select pixels of at least one of the rows of pixels (Figure 4 shows that the period of clocks CL1 and CL3 are synchronized with the scan driver for producing the selection of pixels as shown by the pulses on gate lines GL1 through G516 in the Figure.).

Regarding claim 7, Nitta et al. disclose the display device according to claim 11, wherein:

the scan driver sequentially selects one row of pixels in response to the second clock signal and selects the pixels twice for each row at a period of one frame in response to the scanning start signal (Figure 4 shows that that the gate lines are sequentially selected according to clock signal CL1 and Figure 10 shows that each gate line is selected twice in a frame period, as indicated by the two gate pulses.);

the scan driver selects n rows of pixels at timing generating signal just before the timing at which the second clock signal is not created (Figure 4 shows that 4 rows are selected when clock signal CL3 is not created.);

the data driver supplies the tone voltage corresponding to the display data to the pixels of one row in response to the first clock signal (Figure 4 shows that in accordance with clock signal CL1 display data is supplied one row at a time to rows G513 through G516.); and

the data driver supplies the tone voltage corresponding to the blanking data to the pixels of n rows (Figure 4 shows that blanking data B shown in signal O-DDR is supplied to the 4 rows G1 through G4.).

Regarding claim 8, Nitta et al. disclose the display device according to claim 11, wherein the control circuit outputs to the scan driver a first scanning enable signal to invalidate selection of the pixels by the scan driver at timing generating signal just

before the timing at which the second clock signal is not created and a second scanning enable signal to validate selection of the pixels by the scan driver at timing generating signal just before the timing at which the second clock signal is not created (Figure 4 shows signals DISP1 through DISP3. Column 24, lines 3-25 explain that DISP1 makes it possible to validate selection of pixels by the scan driver when CL3 is not created, where as signals DISP2 and DISP3 invalidate the selection during the period when CL3 is not created).

Regarding claim 12, Nitta et al. disclose the display device according to claim 11, wherein:

the scan driver selects the pixels of one row in response to the second clock signal and the scanning start signal during a period of time from a horizontal scanning period starting at timing at which the second clock signal is created immediately before the timing at which the second clock signal is not created to a horizontal scanning period starting at timing at which the second clock signal is not created (Figure 4 shows that before CL3 is not created that FLM is supplied and lines G513 through G56 are selected before CL3 is not created.); and

the scan driver selects the pixels of n rows during one horizontal scanning period at which the second clock signal is created immediately before the timing at which the second clock signal is not created (Figure 4 shows that 4 rows G1 through G4 are selected immediately before CL3 is not created.).

Regarding claim 13, Nitta et al. disclose the display device according to claim 12, wherein:

the data driver supplies to the pixels the tone signal corresponding to the display data in response to the first clock signal during a horizontal scanning period starting at timing at which the second clock signal is created immediately before the timing at which the second clock signal is not created (Figure 4 shows that O-DDR has display data that is supplied during a time before CL3 is not created); and

the data driver supplies to the pixels the tone signal corresponding to the blanking data during a horizontal scanning period starting at timing at which the second clock signal is not created (Figure 4 shows that O-DDR has blanking data B that is supplied during a time when CL3 is not created.).

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

15 August 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER